Remarks

Claims 1-10, and 12-20 are pending.

Claim 11 is cancelled.

Claims 1-10, and 12-20 are rejected.

Claim Amendments

Claims 2, 6, 9, 13, and 18 have been amended, adding further details of the bridging circuit. Support for the amendments may be found in the application, for example, on page 6 and FIG. 4. Claims 1, 8, 12, 14, and 18 have been amended, adding details of a state machine. Support for the amendments may be found in the application, for example, on page 6. Claim 5 has been amended to correct a grammar error.

No new matter has been added.

Specification Amendments

A paragraph has been added to page 6 describing the coupling of blocks as illustrated in the original FIG. 4. A paragraph on page 6 has been amended to clarify "the remaining chip components." No new matter has been added.

Drawing Amendments

FIG. 4 has been amended to add reference numerals to various blocks as described in the specification as amended. No new matter has been added.

References Cited

The Examiner has cited various non-patent documents such as "USB in a nutshell", "Advanced Technology Attachment (ATA)" Wikipedia entry, and "Designing a Robust USB Serial Interface Engine (SIE)". The Examiner is reminded that the present application was filed

on November 16, 2001 and claims priority to a provisional application filed on November 17, 2000.

However, as far as the Applicant can determine, "USB in a nutshell" has a date of November 23, 2002, more than a year after the filing date of the present application and more than two years after the filing date of the provisional application.

The earliest version of the ATA Wikipedia entry the Applicant has found is attached as Exhibit A. This version was dated February 2002, three months after the filing date of the present application and fifteen months after the filing date of the provisional application.

No date can be found on the "Designing a Robust USB Serial Interface Engine (SIE)".

The USB Specification, Revision 2.0 has a date of April 27, 2000, only seven months before the filing date of the provisional application..

The Applicant requests that the Examiner clarify the usage of the above references, including explaining if the Examiner believes the references are prior art and providing publication dates for such references.

In addition, in the rejections of claims under 35 USC 103, the Examiner has referenced the Application, including page 2 describing the Summary of the Invention, and FIGs. 2 and 3. The Examiner is reminded that a judgment on obviousness is proper so long as it takes into account only knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made and does not include knowledge gleaned only from the applicant's disclosure. *See MPEP 2145 X. A.*. The Examiner cannot rely on the cited portions of the application to support a rejection under 35 USC 103 as it is impermissible hindsight.

Claim Rejections

Claims 1-20 were rejected under 35 USC 102(e) as being anticipated by Kobayashi (U.S. Patent No. 6,199,122). Claims 5, 9-11, 17, and 20 were rejected under 35 USC 103(a) as being unpatentable over Kobayashi. Claim 12 was rejected under 35 USC 103(a) as being unpatentable over Kobayashi, as applied to claims 9-11 above, and further in view of USB 2.0 Specification.

As amended, claims 2, 6, 9, 13, and 18 include an input/output interface coupled to the serial interface engine, a ram control circuit coupled to the input/output interface, a global control circuit coupled to the input/output interface, a translate circuit coupled to the global control circuit; and a disk interface coupled to the ram control circuit and the translate circuit.

Kobayashi does not teach such an input/output interface, a ram control circuit, a global control circuit, or a translate circuit coupled as described above. Accordingly, claims 2, 6, 9, 13, 18 and dependent claims 7-8, 10, 12, 14-17, and 19-20 are allowable under 35 USC 102(e) over Kobayashi.

The combination of Kobayashi and the USB 2.0 Specification does not teach or suggest such an input/output interface, a ram control circuit, a global control circuit, or a translate circuit coupled as described above. Thus, claims 2, 6, 9, 13 and dependent claims 7-8, 10, 12, 14-17, and 19-20 are patentably distinguishable over the combination of Kobayashi and the USB 2.0 Specification. Accordingly, claims 2, and 6-20 are allowable under 35 USC 103(a) over the combination of Kobayashi and the USB 2.0 Specification.

In addition, as amended claims 1, 8, 12, 14, and 18 include a state machine to translate the ATA/ATAPI signals into USB signals in response to embedded commands in the

ATA/ATAPI signals, or similar structures or methods. Although Kobayashi mentions an idle state and a stalled state, no translation or conversion of the ATA/ATAPI signals into USB signals is performed in response to a state machine responsive to embedded commands in the ATA/ATAPI signals.

Kobayashi does not teach such a state machine responsive to embedded commands in the ATA/ATAPI signals as described above. Accordingly, claims 1, 8, 12, 14, 18, and dependent claims 2-5, and 19-20 are allowable under 35 USC 102(e) over Kobayashi.

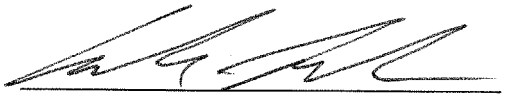
The addition of the USB 2.0 Specification does not cure the deficiencies of Kobayashi. As a result, the combination of Kobayashi and the USB 2.0 Specification does not teach or suggest each and every element of claims 1, 8, 12, 14, 18, and dependent claims 2-5, and 19-20. Accordingly, claims 1-5, 8, 12, 14, and 18-20 are allowable under 35 USC 103(a) over the combination of Kobayashi and the USB 2.0 Specification.

For the foregoing reasons, reconsideration and allowance of claims 1-10, and 12-20 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	19	20*		x $50 =	$ -0-
Independent Claims	5	5**		x $200 =	$ -0-
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$ -0-

*greater of twenty (20) or number for which fee has been paid
**greater of three (3) or number for which fee has been paid

☒ Any deficiency or overpayment should be charged or credited to deposit account number 13-1703.

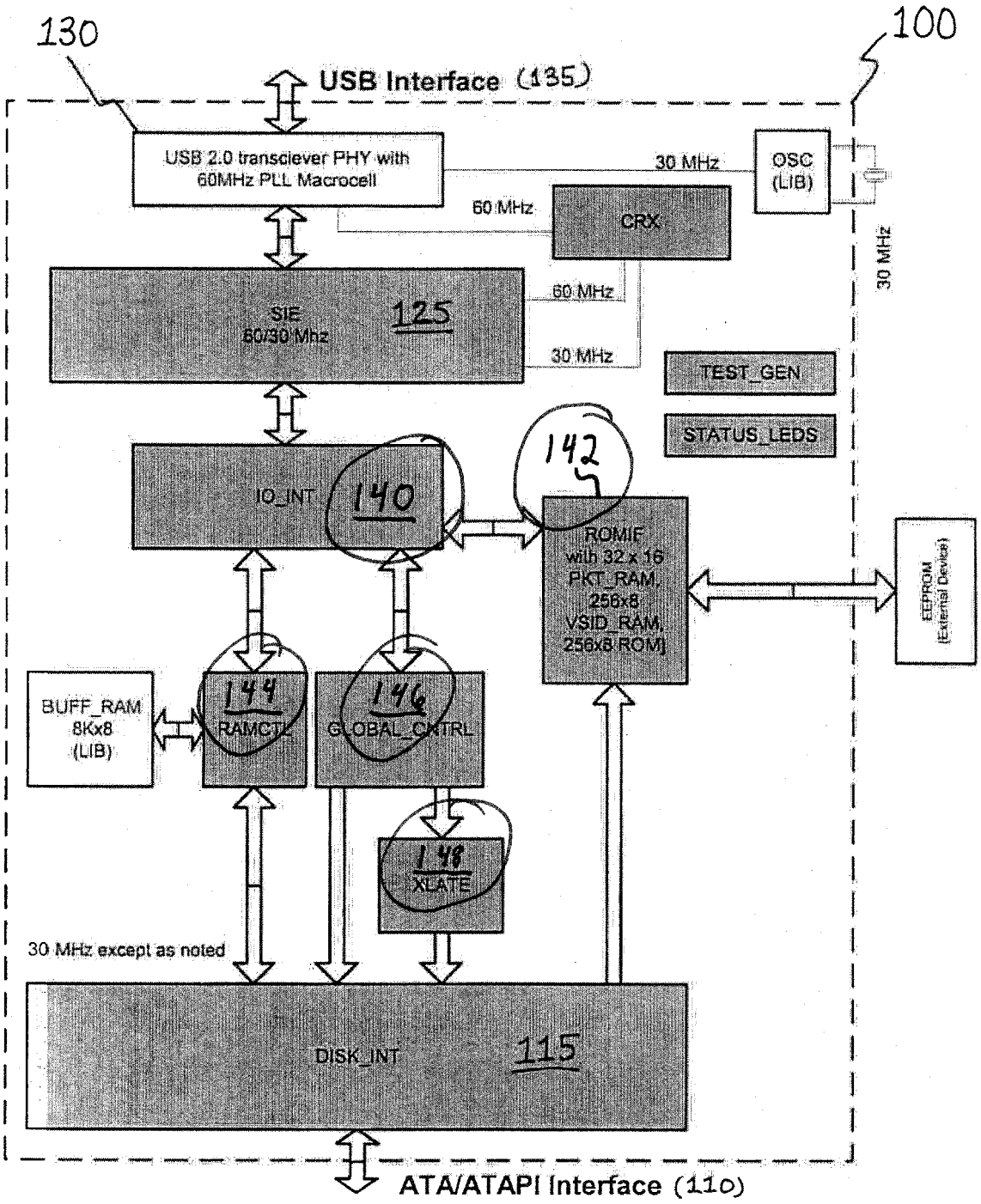
130
100
USB Interface (135)
USB 2.0 transciever PHY with 60MHz PLL Macrocell
30 MHz
OSC (LIB)
60 MHz
CRX
30 MHz
SIE 60/30 Mhz
125
60 MHz
30 MHz
TEST_GEN
STATUS_LEDS
142
IO_INT
140
ROMIF with 32 x 16 PKT_RAM, 256x8 VSID_RAM, 256x8 ROM)
EEPROM (External Device)
BUFF_RAM 8Kx8 (LIB)
144
RAMCTL
146
GLOBAL_CNTRL
148
XLATE
30 MHz except as noted
DISK_INT
115
ATA/ATAPI Interface (110)

FIG. 4